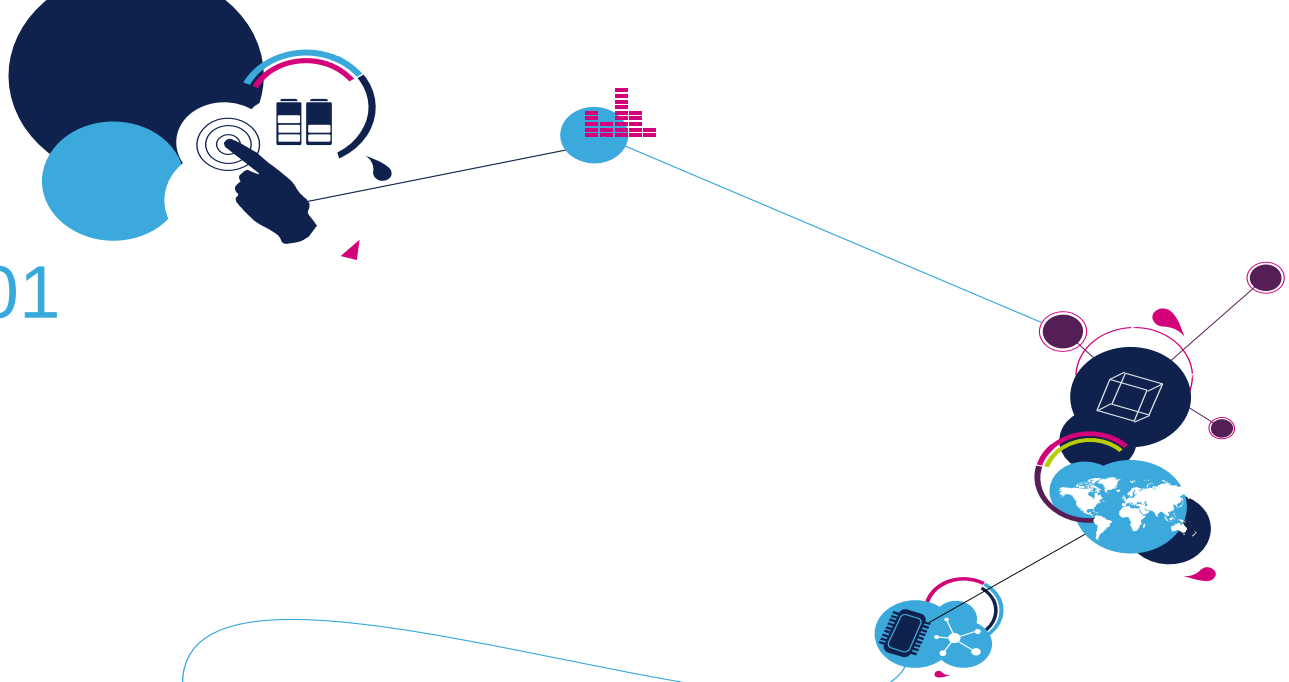
MV5W – VIper01



UAW7 BCD8sp CATANIA
+
VA8P SuperMesh1 AMJ9
Assembled in SSOP10L TSHT CHINA

life.augmented

IPC Product / Quality & Reliability
16-05-2018 Author: A. Spiezia Appoved G. Capodici

TEST	Assy LOT#1	Assy LOT#2	Assy LOT#3
PRECONDITIONING JEDEC MSL 3 (192h 30°C/60%H.R.) REFLOW PROFILE	**JL3: 0rej**	**JL3: 0rej**	**JL3: 0rej**
TC – Temperature Cycling Conditions: 500cy -65°C/+150°C Preconditioning Before	**25ss** **200cy: 0rej**	**25ss** **200cy: 0rej**	**25ss** **200cy: 0rej**
AC – AutoClave (Pressure Pot) 121°C/ 2atm/ 96h Preconditioning Before	**25ss** **96h: 0rej**	**25ss** **96h: 0rej**	**25ss** **96h: 0rej**
HTSL – High Temperature Storage Life Tj=Ta=150°C (no bias) , 1000H	**25ss** **500h: 0rej**	**25ss** **500h: 0rej**	**25ss** **500h: 0rej**

TEST	Assy LOT#1
ESD (CDM)	3ss Passed 750V

PRELIMINARY RELIABILITY EVALUATION

QUALIFICATION TRANSFER OF:

UE40 /L4984DTR

ASSEMBLED ON SSOP10L SINGLE DIE
FROM ST-BSK (MOROCCO)
TO
TSHT SUBCON (CHINA)

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	17-May-2018		F.VENTURA AMS/I&PC QA&R / B/E	A.PLATINI AMS/ I&PC QA&R MNG.	Preliminary report

General Information	
Product Line	*99W4*UE40BE6*
P/N	*L6564D*
Product Group	*AMS*
Product division	*Industrial & Power Discrete*
Package	*SSOP10L .150 NARROW*
Silicon Process technology	A7 - BCD2S 2Q - BCD60IISDM-D (19/2m)
Maturity level step	*21*

Locations	
Wafer fab	AM6F-Singapore 6"
Assembly plant	Z9LA SC-Tianshui Huatian-China (TSHT) 999L
Preliminary Reliability Assessment	*PASSED*
Reliability Lab	Z9LA SC-Tianshui Huatian-China (TSHT) 999L

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
ADCS:8161393	General specification for product development

1 GLOSSARY

DUT	Device Under Test
SS	Sample Size

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

To qualify new **TSHT SUBCON MANUFACTURING PLANT** Transferring ST- AMS/I&PC product.

2.2 Conclusion:

Basis on the achieved positive data , Preliminary RR report can be issued.
Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is onsequently expected during their lifetime.

2.3 Construction note

	***UE40 _ P/N:** *L6564D*
Wafer/Die fab. information	AM6F
Wafer fab manufacturing location	AM6F-Singapore 6"
Technology	A7 - BCD2S
Process family	2Q - BCD60IISDM-D (19/2m)
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die size	1790,2450 um
Bond pad metallization layers	AlSiCu
Passivation type	P-VAPOX(SiO2) / NITRIDE (SiN)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	TSHT
Assembly information	
Assembly site	Z9LA SC-Tianshui Huatian-China (TSHT
Package description	W4 SSOP 10L 3.9 BODY 1 PITCH
Molding compound	RESIN Hitachi CEL-9220HF10TS
Frame material	SSOP(1.0) 010
Die attach process	EPOXY GLUE
Die attach material	Henkel 8200T
Die pad size	90x115 std Ag-Ring
Wire bonding process	THERMOSONIC
Wires bonding materials/diameters	Heraeus Au 1.0 mil
Lead finishing process	Sn100%
Package code	W4
Final testing information	
Testing location	TSHT

TESTS RESULTS SUMMARY

2.4 Test vehicle *UE40

Lot #	Diffusion Lot	Assy Lot	Trace Code	Process/ Package	Product Line	Comments
1	**V6732X3J**	**SSO010180307543**	**E7WN3J2V**	**W4 SSOP 10L 3.9**	***99W4*UE40BE6***	

Detailed results in below chapter will refer to P/N and Lot #.

2.5 Test plan and reliminary results summary

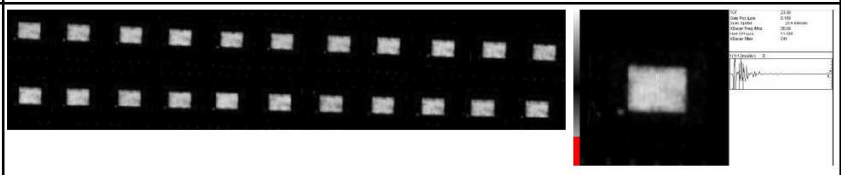
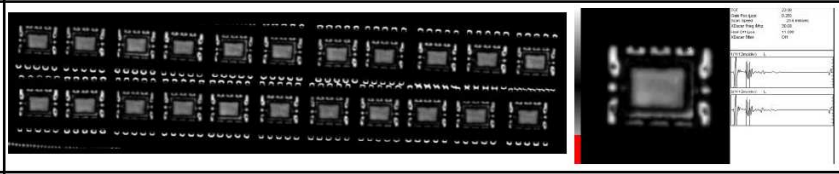
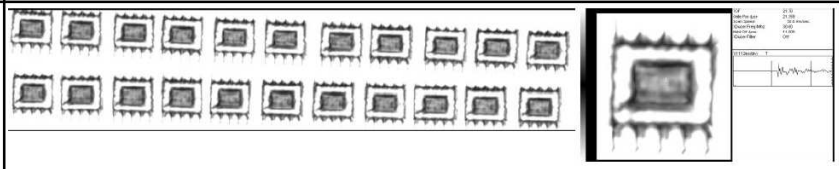
P/N : ***L6564D***

Test	PC	Std ref.	Conditions	Steps	Note	
PC	Y	JESD22 A020-D	MSL_3 (192H 30°C/60%H.R)	0/300	NO DELAMINATION TOP/BOTTOM	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	96H	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	200CY	0/77	
				500CY	0/77	
HTSL	N	JESD22 A-103	Ta = 150°C	500H	0/77	
				1000H	0/77	
THS	Y	JESD22 A-101	85°C/85%RH	168H	0/77	
				500H	0/77	
				1000H	Wk/22	
ESD-CDM	N	AEC Q100011	750V	3ss Wk21-18		
(L-UP) 85°c	N	EC Q100 004	Current Inj. Overvoltage ±100MA	3ss Wk21-18		

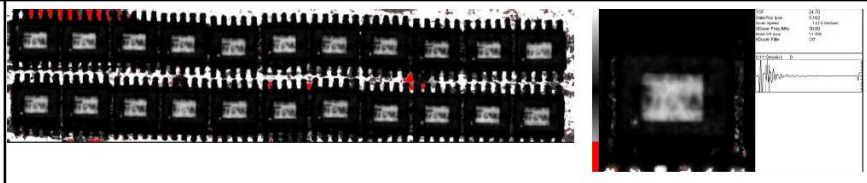
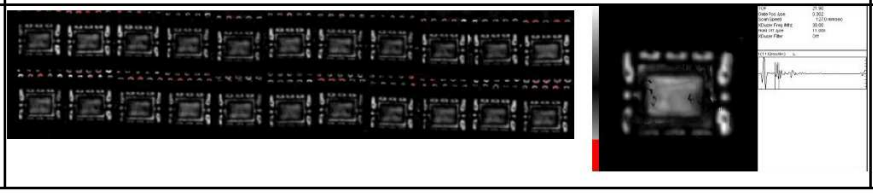
2.6 SAM PICTURE :

Annex I: SAM Picture:

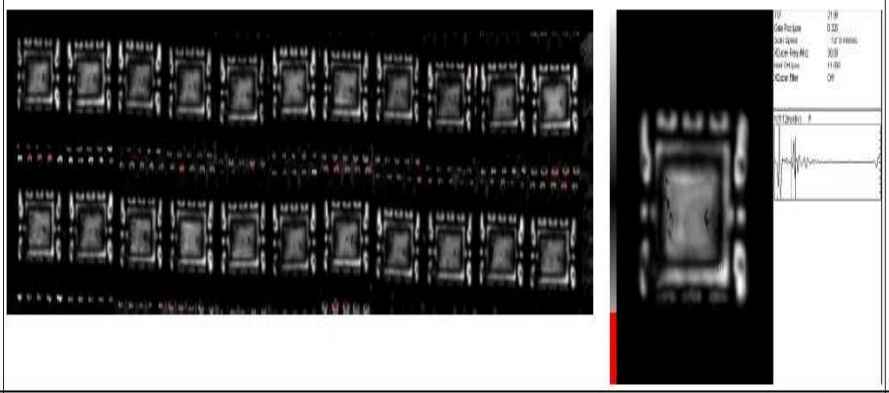
➢ Before Test

聚焦界面 (Focus side)	扫描图片(SAM pictures)	扫描结果 (SAM result)
DIE		22 只样品芯片聚焦扫描，无分层现象. 22pcs focused on die,no delamination;
LEAD		22 只样品管腿聚焦扫描，无分层现象. 22pcs focused on lead, no delamination;
PAD		22 只样品载体聚焦扫描，无分层现象. 22pcs focused on paddle, no delamination;
T-SCAN		无异常 T-scan passed

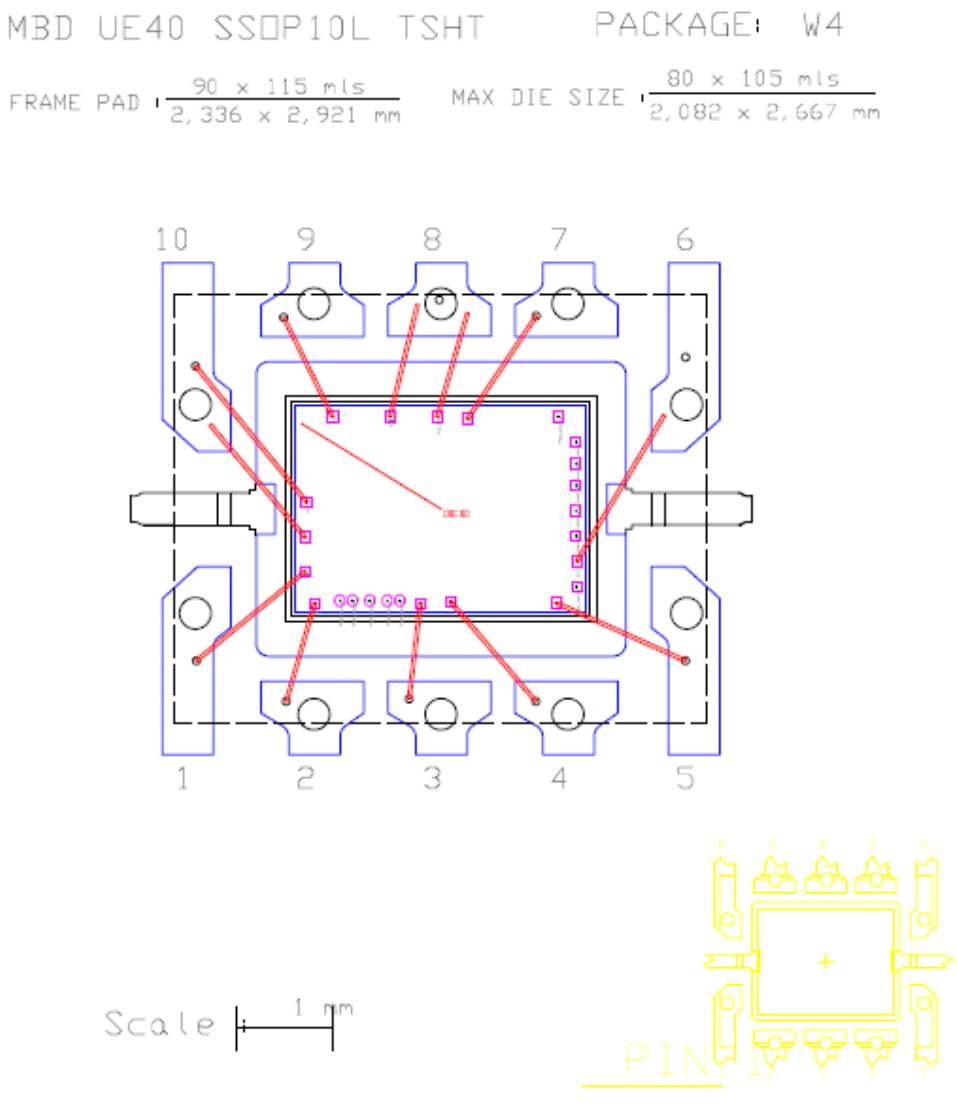
➢ After MSL3:

聚焦界面 (Focus side)	扫描图片(SAM pictures)	扫描结果 (SAM result)
DIE		22 只样品芯片聚焦扫描，无分层现象. 22pcs focused on die, no delamination;
LEAD		22 只样品管腿聚焦扫描，无分层现象. 22pcs focused on lead, no delamination;

HUA TIAN

	PAD		22 只样品载体聚焦扫描，无分层现象. 22pcs focused on paddle, no delamination;
			

.2. ANNEXES: MOUNT BOND DIAGRAM (MBD)



2.6.1 Package outline/Mechanical data

PACKAGE OUTLINE ASSEMBLY

TITLE : POA SSOP 10L 3.9 BODY 1 PITCH

PACKAGE CODE: W4
PLANT CODE: 64BA
PACKAGE WEIGHT: 0,084 g /unit Typ
JEDEC/EIAJ REFERENCE NUMBER: OUT JEDEC MO-137

DIMENSIONS				
REF. DIM	DATA BOOK (mm)			NOTES
	NOM	MIN	MAX	
A	-	-	1.75	
A1	-	0.10	0.25	
A2	-	1.25	-	
b	-	0.31	0.51	
c	-	0.17	0.25	
D	4.90	4.80	5	
E	6	5.80	6.20	
E1	3.90	3.80	4	
e	1	-	-	
h	-	0.25	0.50	
L	-	0.40	0.90	
K	-	0°	8°	

GENERAL PACKAGE PERFORMANCE

1- **SSOP** standard for Shrink Small **O**utline **P**ackage family.
2- The leads size is comprehensive of the thickness of the leads finishing material.
3- Dimensions do not include mold protrusion, not to exceed 0,15 mm
4- Package outline exclusive of metal burr dimensions.

PACKAGE OUTLINE ASSEMBLY

TITLE : POA SSOP 10L 3.9 BODY 1 PITCH

PACKAGE CODE: W4
PLANT CODE: 999L
PACKAGE WEIGHT: 0.084 g /unit Typ
JEDEC/EIAJ REFERENCE NUMBER: JEDEC MO-272

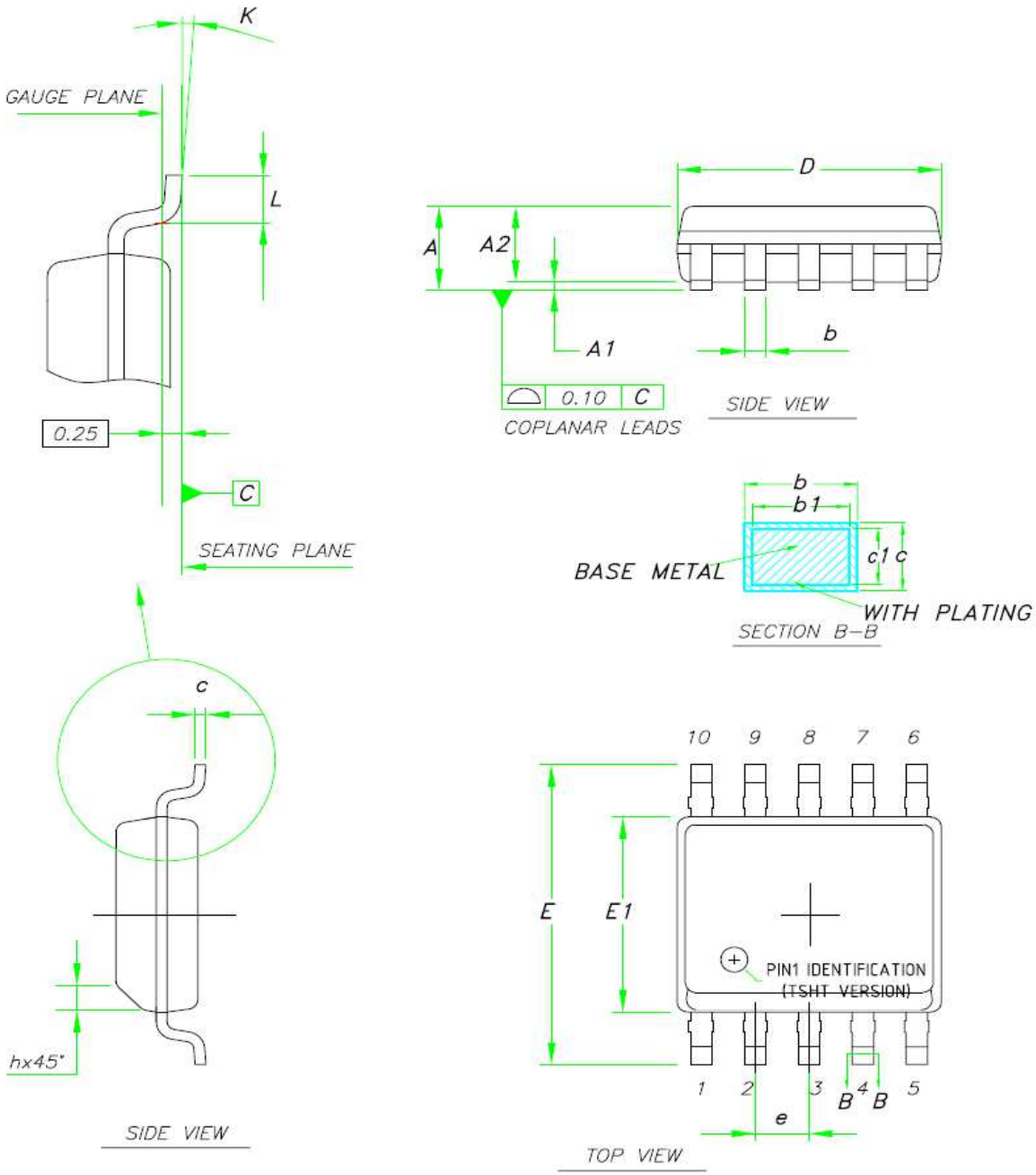
DIMENSIONS				
REF. DIM	DATABOOK (mm)			
	MIN	NOM	MAX	
A	-	-	1.75	
A1	0.10	-	0.225	
A2	1.30	1.40	1.50	
A3	0.60	0.65	0.70	
b	0.39	-	0.47	
b1	0.38	0.41	0.44	
c	0.20	-	0.24	
c1	0.19	0.20	0.21	
D	4.80	4.90	5.00	
E	5.80	6.00	6.20	
E1	3.80	3.90	4.00	
e	1.00 BSC			
h	0.25	-	0.50	
L	0.50	-	0.80	
K	0°	-	8°	

GENERAL PACKAGE PERFORMANCE

1- **SSOP** standard for **S**hrink **S**mall **O**utline **P**ackage family.
2- The leads size is comprehensive of the thickness of the leads finishing material.
3- Dimensions do not include mold protrusion, not to exceed 0,15 mm
4- Package outline exclusive of metal burr dimensions.

PLANT CODE: 64BA, 999L

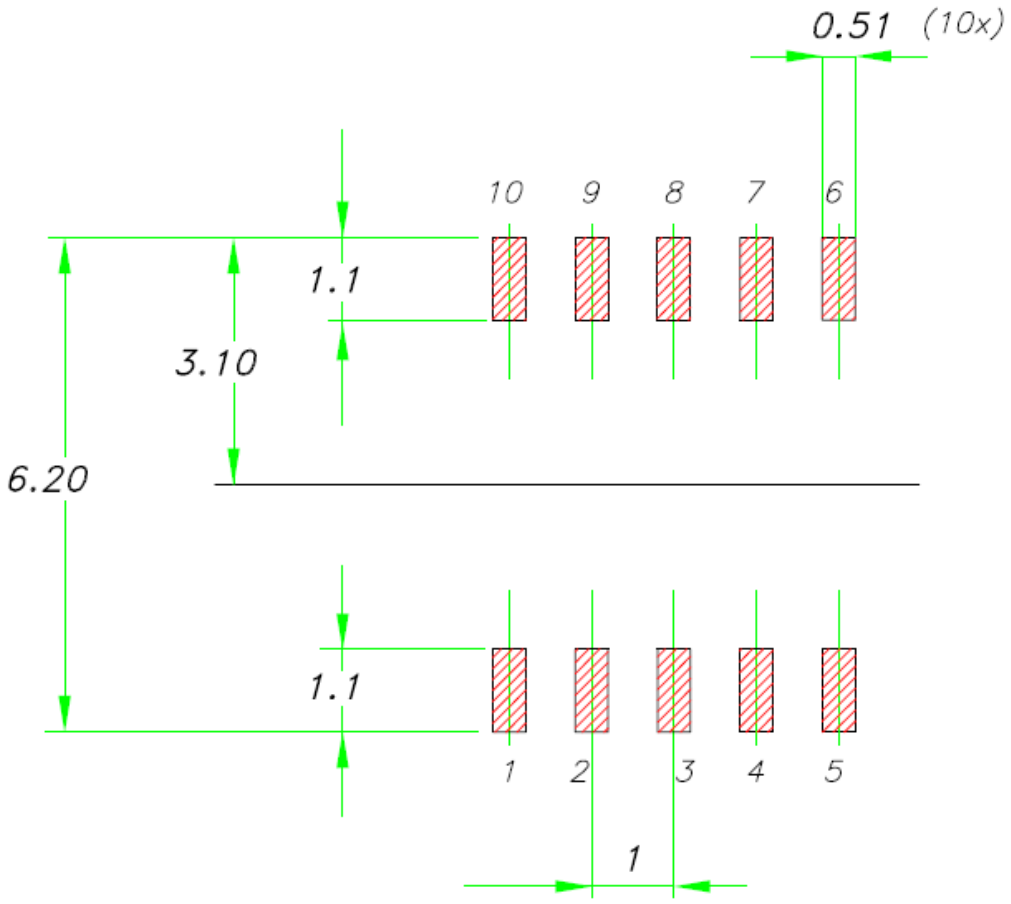
POA SSOP 10L 3.9 BODY 1.0 PITCH



FOOTPRINT SUGGESTED

PLANT CODE: 64BA, 999L

POA SSOP 10L 3.9 BODY 1.0 PITCH



Tests Description

Test name	Description	Purpose
Die Oriented		
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

Reliability Report

General Information	
Product Line	*U1MA*
Product Description	*High Power Factor Flyback controller*
Product division	*I&PC*
Package	*SSOP10*
Silicon process technology	*BCD6S*

Locations	
Wafer fab location	*AGRATE*
Assembly plant location	*TSHT CHINA*
Reliability assessment	*Preliminary*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	16-May-18	11	A. Spiezia	Preliminary release

Approved by
G. Capodici

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement of STMicroelectronics.

Table of Contents

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
0061692	: Reliability tests and criteria for qualifications

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of U1MA device diffused in AGRATE and assembled in SSOP10 in TSHT CHINA in the overall plan of SSOP10 assembly line qualification in TSHT.
According to Reliability Qualification Plan, considering that U1MA assembled in Bouskoura is already qualified and in production, below is the list of the trials performed:

Die Oriented Tests

- High Temperature Operating Life
- Early Life Failure Rate

Package Oriented Tests

- Preconditioning
- Temperature Cycling
- Autoclave
- High Temperature Storage Life
- Temperature Humidity Bias

Electrical Characterization

- ESD resistance test

2.2 Conclusion

The preliminary reliability results have shown that the devices behave correctly against environmental tests. Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation.

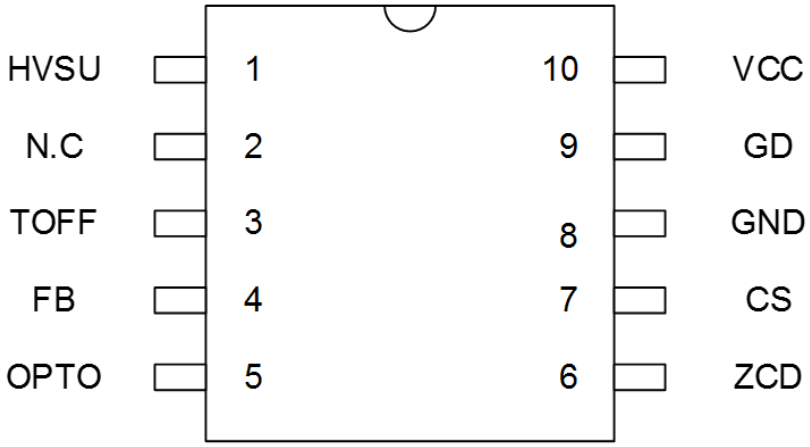
3 DEVICE CHARACTERISTICS

3.1 Device description

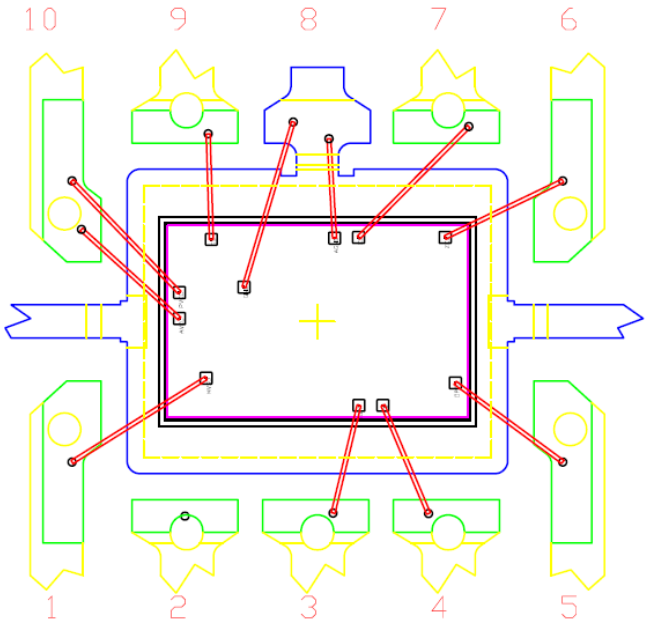
3.1.1 Generalities

The U1MA is an enhanced peak current mode controller able to control mainly high power factor (HPF) flyback or buck-boost topologies in LED drivers having an output power up to 150 W. Some other topologies, like buck, boost and sepic could also be implemented.

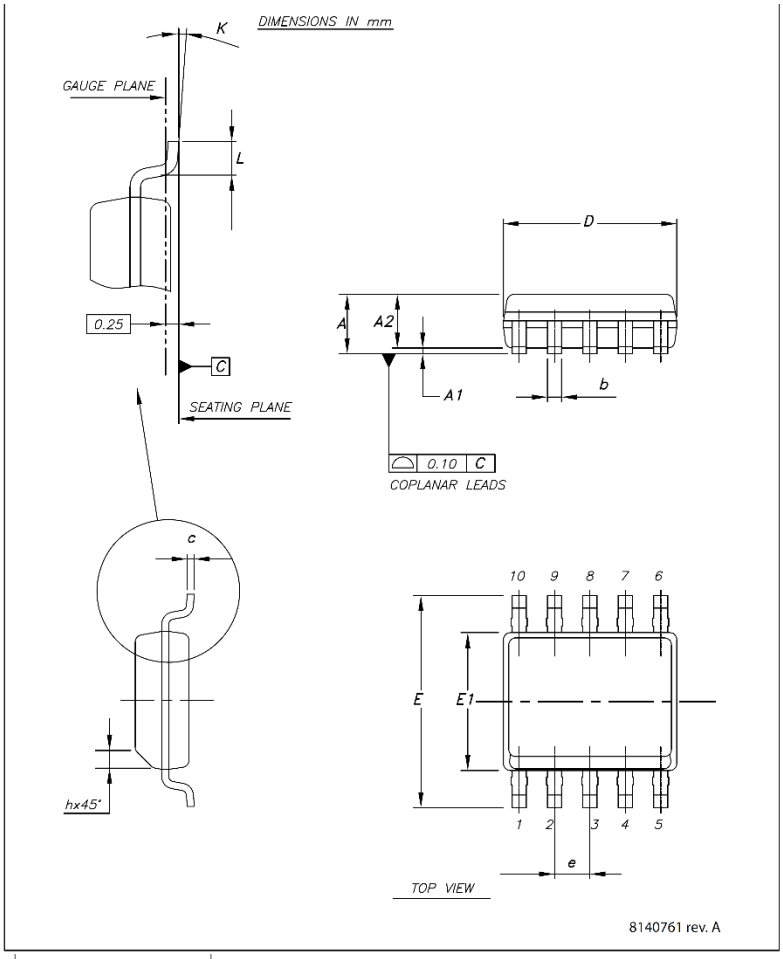
3.1.2 Pin connection



3.1.3 Bonding diagram



3.1.4 Package outline/Mechanical data



Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	4.80	4.90	5
E	5.80	6	6.20
E1	3.80	3.90	4
e		1	
h	0.25		0.50
L	0.40		0.90
K	0°		8°

3.2 Traceability

Wafer fab information	
Wafer fab manufacturing location	*AGRATE*
Wafer diameter	*8inch*
Wafer thickness	*375 um*
Silicon process technology	*BCD6S*
Die finishing back side	*Cr/NiV/Au*
Die size	*1608,2436 UM*
Bond pad metallization layers	*AlCu*
Passivation	*HDP/TEOS/NITRIDE*
Metal levels	*3*

Assembly Information	
Assembly plant location	*TSHT CHINA*
Package description	*SSOP10*
Molding compound	*CEL-9220HF10TS*
Wires bonding materials/diameters	*PdCu 1.2mil*
Die attach material	*8200T*
Lead solder material	*Sn*

4 TESTS RESULTS SUMMARY

4.1 Test plan and results summary

Die Oriented Tests							
Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 1	Lot 2	Lot 3		
HTOL	High Temperature Operating Life						
	PC before	Conditions: Tj=150°C Vhv=480V; Vcc=18V	0/77	-	-	1000h	
ELFR	Early Life Failure Rate						
		Conditions: Tj=150°C Vhv=480V; Vcc=18V	-	0/500	-	48h	

Package Oriented Tests							
Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 1	Lot 2	Lot 3		
PC	Pre-Conditioning: Moisture sensitivity level 3						
		192h 30°C/60% - 3 reflow PBT 260°C	0/210	0/110	0/110		
THB	Temperature Humidity Bias						
	PC before	Ta=85°C/85%RH Vhv=100V; Vcc=18V	0/25	0/25	0/25	500h	To be continued up 1000h
AC	Autoclave						
	PC before	121°C 2atm	0/25	0/25	0/25	96h	
TC	Temperature Cycling						
	PC before	Temp. range: -65/+150°C	0/25	0/25	0/25	500cy	
HTSL	High Temperature Storage						
	No bias	Tamb=150°C	0/25	0/25	0/25	1000h	

Electrical Characterization Tests							
Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 1	Lot 2	Lot 3		
ESD	Electro Static Discharge						
	Charge Device Model	+/- 750V	0/3	-	-		

Electrical Characterization Tests (on SSOP10 Bouskura)					
Test	Method	Conditions	Failure/SS Lot 4	Duration	Note
ESD	Electro Static Discharge				
	Human Body Model	+/- 2kV	0/3		
	Machine Model	+/- 200V	0/3		
	Charge Device Model	+/- 750V	0/3		
LU	Latch-Up				
	Over-voltage and Current Injection	Tamb=85°C Jedec78	0/6		

Tests Description & detailed results

4.2 Die oriented tests

4.2.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

4.2.2 Early Life Failure Rate

This test is to evaluate the defects inducing failure in early life.
The device is stressed in biased conditions at the max junction temperature.

The read-outs flow chart is the following:

- Initial testing @ Ta=25°C
- Final Testing (48 hr.) @ Ta=25°C

4.3 Package oriented tests

4.3.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

4.3.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

4.3.3 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 200 cycles.
- Final Testing @ 500 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -65°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

4.3.4 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (96hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 96 hrs

4.3.5 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 1000 h.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs
- Final Testing (1000 hr.) @ Ta=25°C
-

4.4 Electrical Characterization Tests

4.4.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less
IN high	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less

4.4.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** — ANSI/ESDA/JEDEC STANDARD JES001
  CDF-AEC-Q100-002
- **Machine Model** — JEDEC STANDARD EIA/JESD-A115
  CDF-AEC-Q100-003
- **Charge Device Model** — ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101
  CDF-AEC-Q100-011